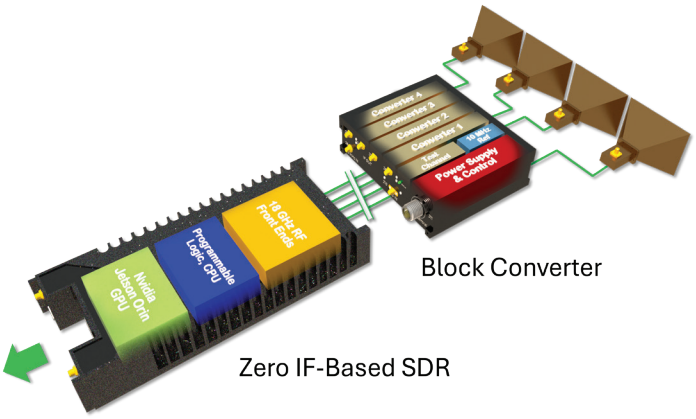
SOFTWARE DEFINED RADIOS – WHICH RF ARCHITECTURE SHOULD I CHOOSE?

Introduction

Software Defined Radios (SDRs) have become ubiquitous in applications that value their flexibility, reconfigurability, spectrum agility and upgradability. These include defense, public safety, wireless infrastructure, space, SATCOM, test and measurement to name a few. However, there are several common methods of implementing SDR architectures – how do you know which is best to meet a specific need? In this paper we will look at some common architectures, their pros and cons, and their likely development trajectories given the levels of investment being poured into them.



Why Should I Care Which SDR Architecture Was Chosen?

When deciding on the best approach to solving a particular RF challenge, there tend to be two competing, orthogonal inputs – Function and Form. Put another way, they can be thought of as desired capabilities and forced constraints, as illustrated in **Figure 1**. They are met with differing degrees of success by the architecture chosen depending on the balance between them and frequently may be met by multiple approaches.

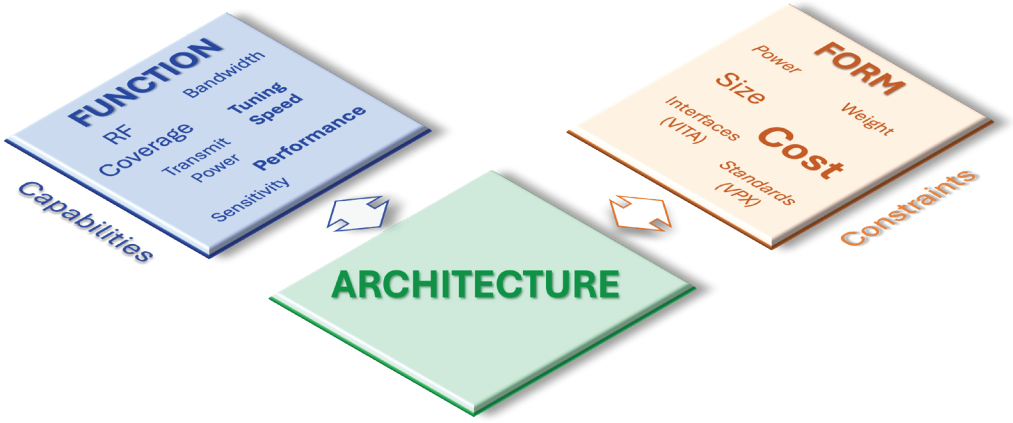


Figure 1: Architecture links the orthogonal axes of desired capabilities and forced constraints.

Common architectures include the following:

1. Superheterodyne, also known as Superhets, Heterodyne, or 2-Stage Heterodyne.
2. Block Converter, also known as Downconverters/ Upconverters, or 1-Stage Heterodyne.
3. Direct Sampling, which is sometimes called Direct RF, or Direct RF sampling.
4. Zero IF, also referred to as ZIF, Homodyne, confusingly Direct Conversion, or in some contexts, RFIC.
5. Combined Architectures, which usually involve adding a block converter in front of one of the others.

Simplified representations are shown in **Figure 2**. A few notes:

- For simplicity we're showing the receive side of the signal chain, but the transmit is similar in reverse.
- We don't plan to discuss these in detail as we're focusing on relative trade-offs for particular applications in this paper – more in-depth reading can be found in the References section at the end.
- For the record, we employ all of these architectures and use each of them in particular products that make best use of their advantages, and we engineer around their disadvantages for a given application.
- Super Het and Block Converters require more investment in RF engineering skills, whereas the higher numbered items require a similarly heavy investment but on the digital/ DSP side.

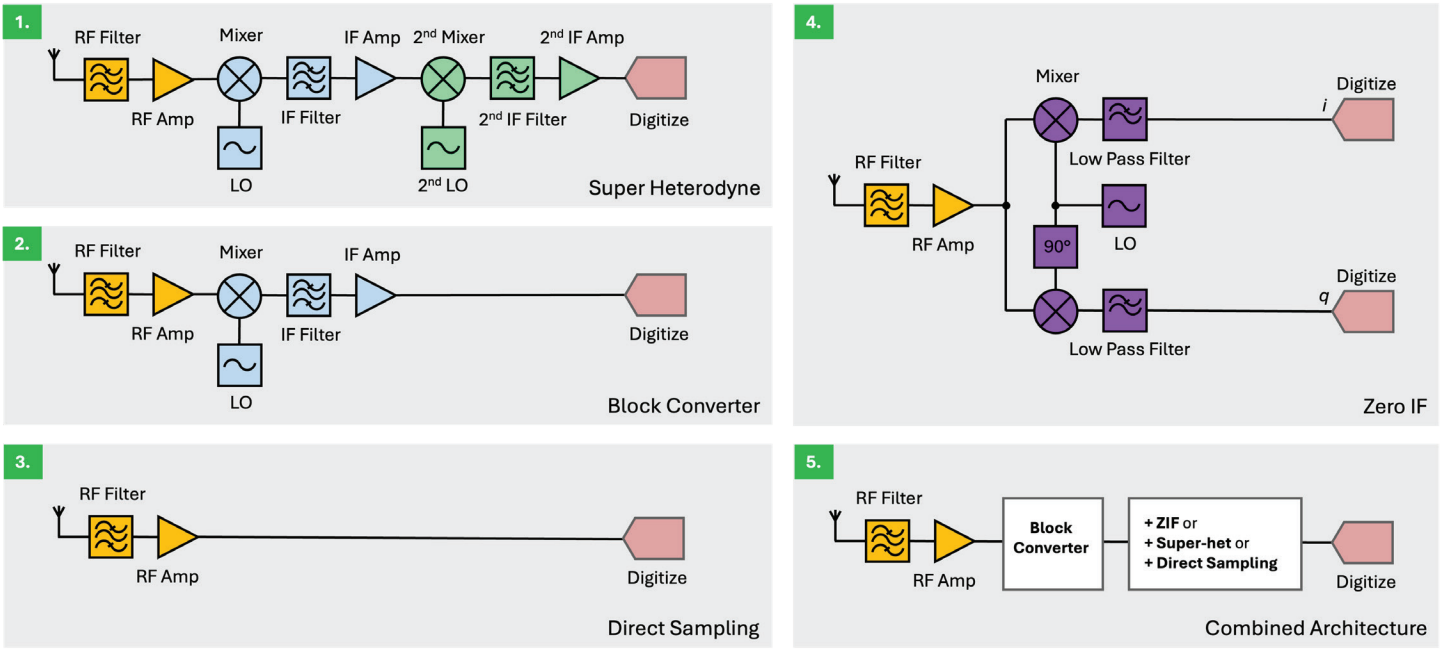


Figure 2: *Five typical SDR architectures*

How do we Assess RF Architectures?

For this exercise we've boiled down the two axes of function and form into the following for simplicity.

RF Function, or Capabilities

- **RF Coverage** – gap-less frequency range that a radio can be tuned to. On the high end, 6 GHz is often available, although for some applications much higher is highly desirable.
- **Bandwidth** – Once tuned to a specific frequency, the width of the frequency band that can be passed through the analog components unattenuated and then digitized at a sufficient sample rate. Example: 100 MHz
- **Performance** – spurious-free dynamic range (SFDR) is used as the primary figure of merit for system performance in this article, though key performance indicators vary depending on application (e.g., see Reference 1).
- **Selectivity** – for many radio applications, having great performance is meaningless if the environment it operates in causes the performance to break down. Selectivity specifies how well RF noise outside the frequency band of interest is attenuated.

Form, or Constraints

If the radio can be infinitely large, infinitely expensive, and be supplied with infinite power, great performance is easy, but this is obviously wholly unrealistic. The parameters are therefore:

- **Size, Weight** and **Power** (SWaP) – smaller is better for each.
- **Reconfigurability** – How easy is it to adapt the design to a different use? Frequency band? IBW?
- **Industry Investment** – we thought it would be interesting to see which architectures are seeing increased investment, deployment, and capabilities for applications such as 5G and automotive radar vs. those that are more niche, as this impacts where to place development effort that will pay off in the future.

For **Function** and **Form** we kept things simple and used a 3-point scale of Poor, Good and Best, as this was sufficient to tease out key differences between each.

Assessing Each Architecture

Architecture 1: Superheterodyne

Description	Superhet selects an RF signal of interest, and after two (and sometimes three) stages of filtering and frequency conversion, digitizes it at baseband.
Primary Benefit	Provides the highest level of performance & customization.
Primary Cost	Generally, is highest for Size, Weight, Power and Cost (SWaP-C).

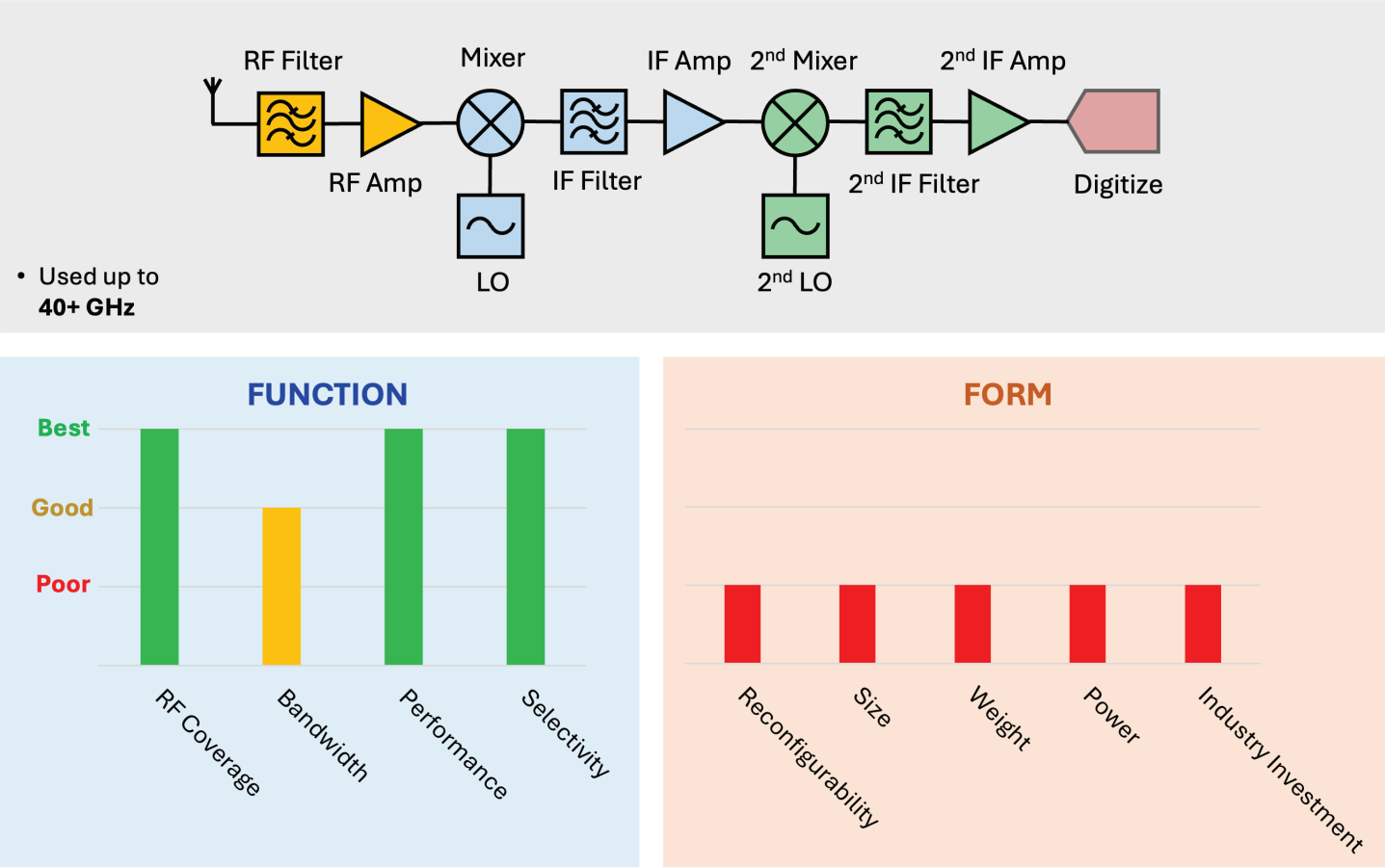


***Figure 3**: Form and Function for Superheterodyne architectures*

As mentioned before, the heavy lifting for this architecture is mostly in exquisite RF expertise. In pure functionality it is hard to beat a Superhet in all-out RF capabilities and performance, including in extremely challenging RF environments with large amounts of strong adjacent signal clutter. With two, or sometimes three conversion stages to ensure the best rejection and filtering, and many discrete components that can be tweaked and optimized for particular objectives, they provide the ultimate in tailoring to extract every ounce of performance; for example, by choosing the best amplifier for a particular place in the conversion chain, the best filter shape for another place, and the exactly the right level to drive a mixer at. They can be designed to go beyond 40 GHz tuning range, and enable IBWs of 500 MHz, 1 GHz or higher. In an RFIC, these choices are made for you by the chip designer.

The penalties come in Size, Weight and Power as well as Cost (SWaP-C), as discrete microwave components tend to be large, heavy and power hungry. All that tweaking and tailoring also makes them complicated to reconfigure for a different task. In general, industry investment in Superhets is low. An example of the complexity involved is shown in **Figure 4**, along with some of many example products made by Epiq that use this architecture.

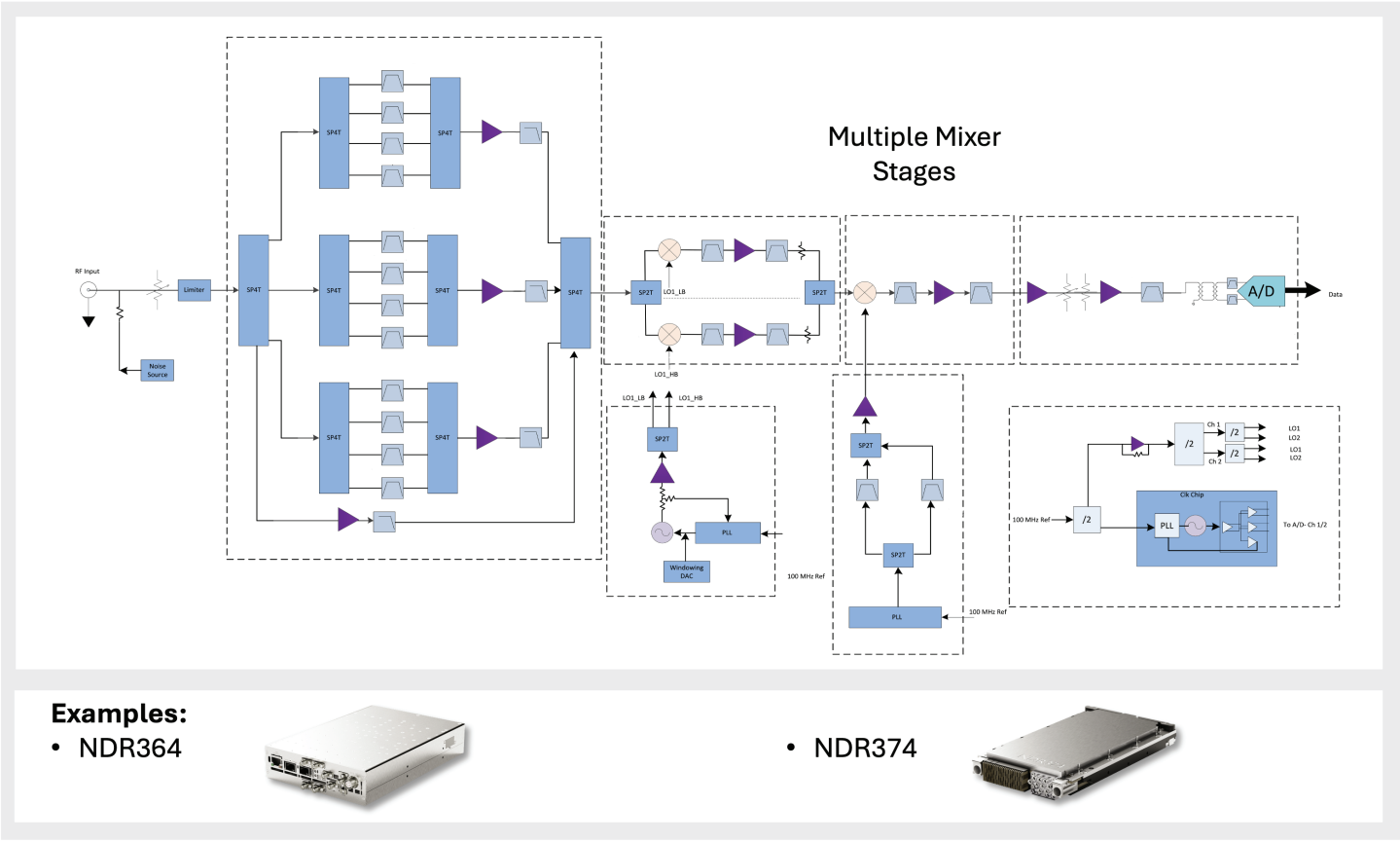


***Figure 4**: Example Superhet block diagram and some of many Epiq products based on a Superhet architecture.*

Architecture 2: Block Converters

Description	Block conversion is similar to Superhet, but only has a single stage of filtering & RF conversion before passing the signal to digitization.
Primary Benefit	Can provide some Superhet attributes for lower SWaP-C. Good for frequency extension.
Primary Cost	Fewer levers for performance optimization.

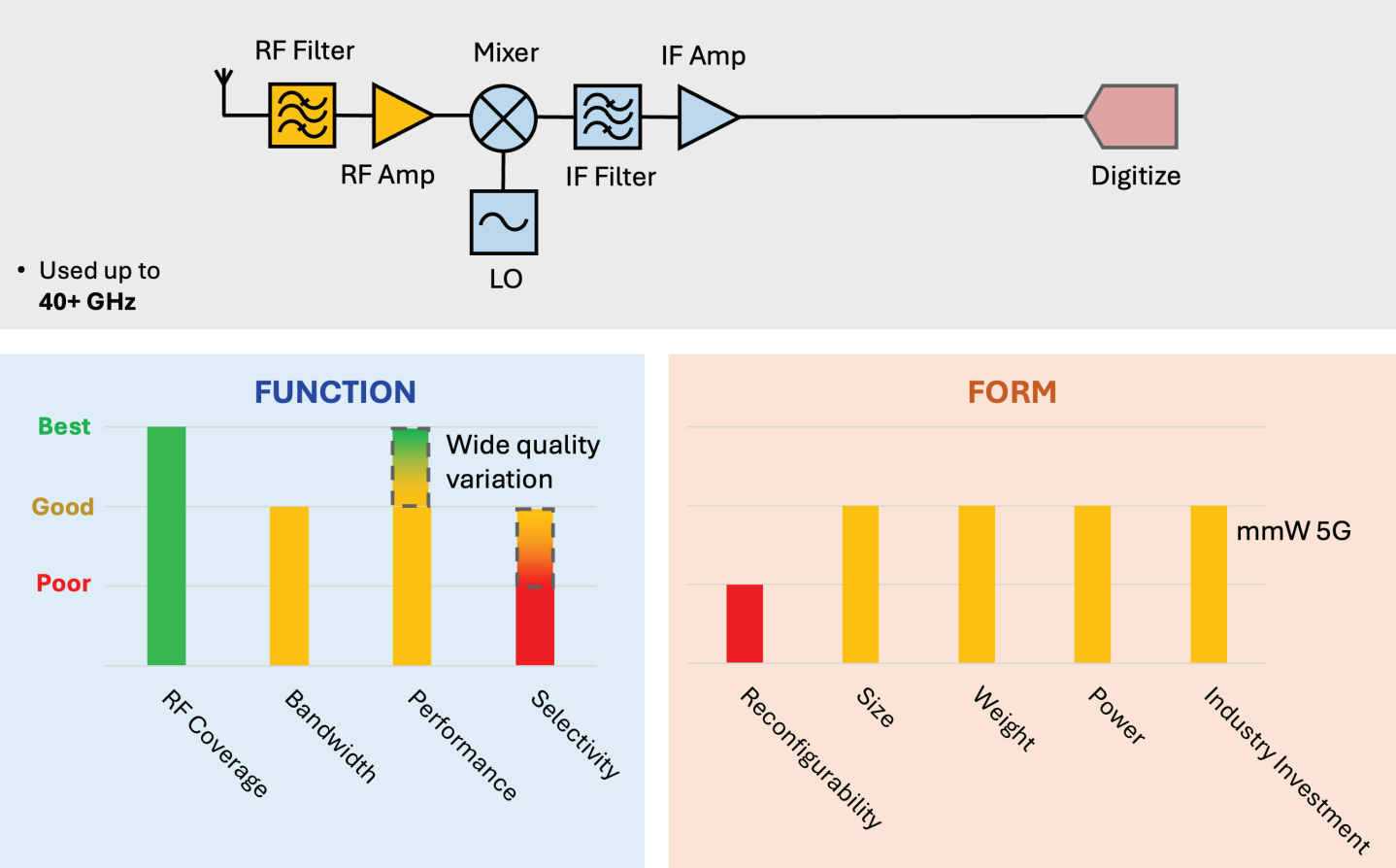


Figure 5: Form and Function for block converter architectures.

Using only a single stage of IF conversion, block converters are both simpler to implement but also have fewer opportunities for performance optimization through the tweaking of individual components than Superhets do (**Figure 6** shows a real example of how block converters are simpler than Superhets). This can lead to a wide variation in the quality of RF performance such that care should be taken in selection. They are often used for down conversion to extend the frequency range of a system, as we will see later. They are commonly designed to operate of a specific narrow range of interest such as 5G millimeter wave bands, and this is the cause of some industry investment currently. Their simplicity means that they can be smaller, lighter and less power hungry than Superhets. However, they usually require an external digitizer to supply the rest of the system with IQ data.

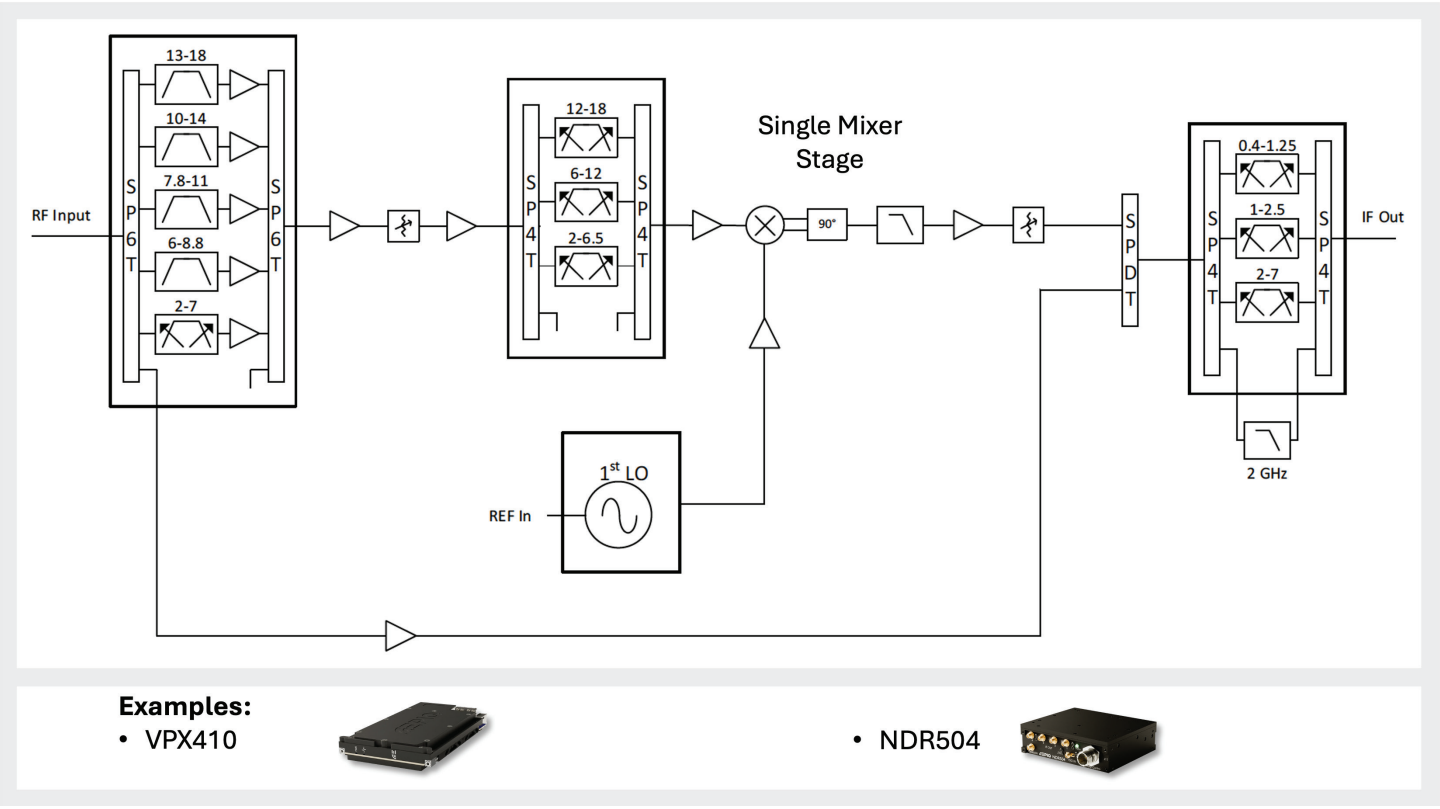
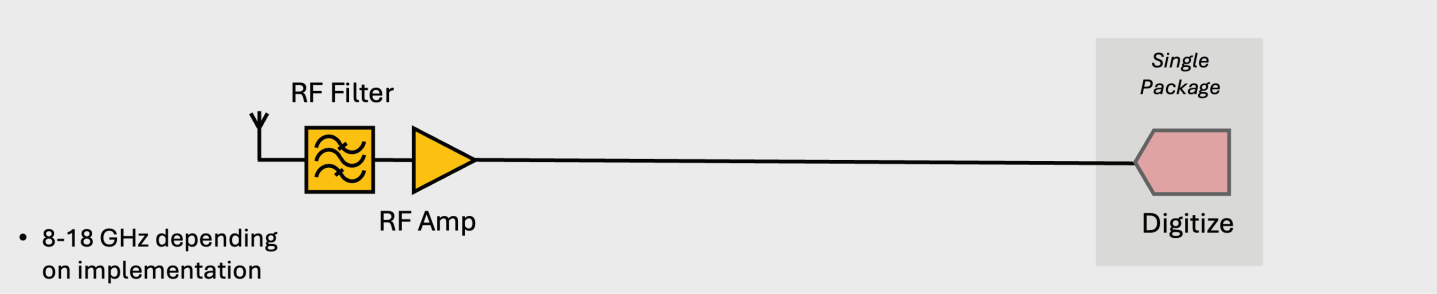
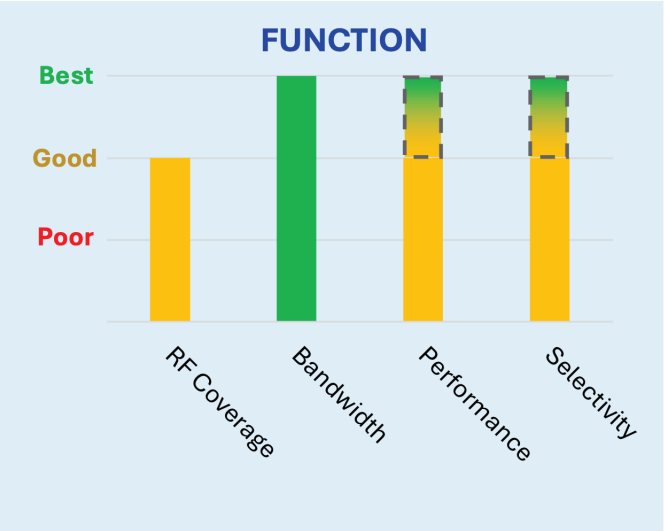


***Figure 6**: Example block converter block diagram showing reduced complexity compared to a Superhet, and two example Epiq products based upon this architecture.*

Architecture 3: Direct Sampling

Description	Direct sampling digitizes the RF signal at RF frequency, without any conversion or IF stages.
Primary Benefit	Is the most digitally defined architecture, analog RF through to IQ data stream.
Primary Cost	Performance is limited by the data converter.





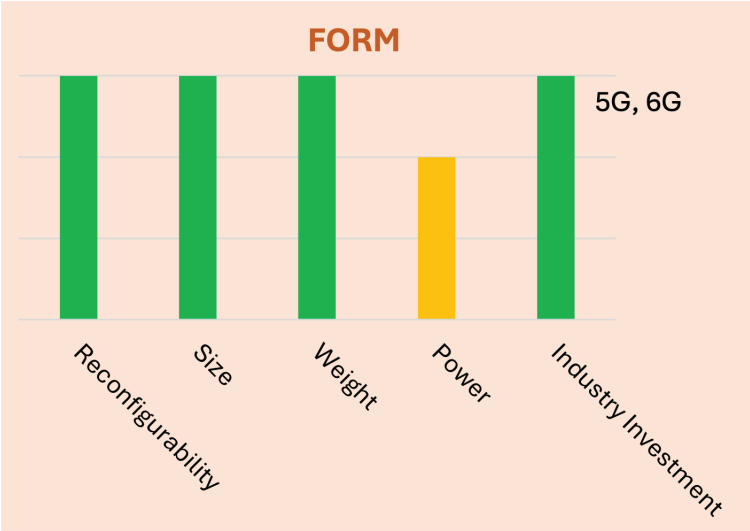


Figure 7: Form and Function for direct sampling architectures.

It's been the dream of microwave system designers for decades to be able to eliminate almost all RF components and convert GHz signals directly to digital to process directly. The continued investment in high speed ADC and DAC converters has broadened the applications that can leverage Direct RF architectures beyond niche use cases in the lower frequency bands. In a direct RF sampling architecture, the mixing stages described in the two earlier cases described here are eliminated, and the antenna is effectively directly connected to an ADC and DAC that is sampling at 10s of GS/s (10,000 MS/s) and is digitizing multiple GHz of RF bandwidth simultaneously. This digitized sample rate is much higher than the desired channel sample rate (assumed to still be in the 10s to 100s of MS/s) and allows for several benefits including judicious lowering of the noise floor through processing gain, as well as allowing a single RF channel to support many independent digital channels each looking at separate signals. A demonstration of the benefits of processing gain is given in **Appendix A: Direct Sampling and Processing Gain**. Very high sample rates selectively applied to narrower band signals allows radio performance that is starting to get close to older designs of Superhet, although small signals in the presence of large interfering signals are likely to continue to be a problem in the most demanding applications.

Example Epiq products that use direct sampling include the space-focused Xiphos Q8RF and the upcoming Matchstiq V40.

Examples:
- Xiphos Q8RF

- Upcoming Epiq V40

Architecture 4: Zero IF

Description	Zero IF converts the desired signal directly from RF frequency to baseband for filtering and digitization.
Primary Benefit	Is the lowest SWaP-C architecture, very spectrally efficient.
Primary Cost	Bandwidth is limited and performance relies on algorithms.

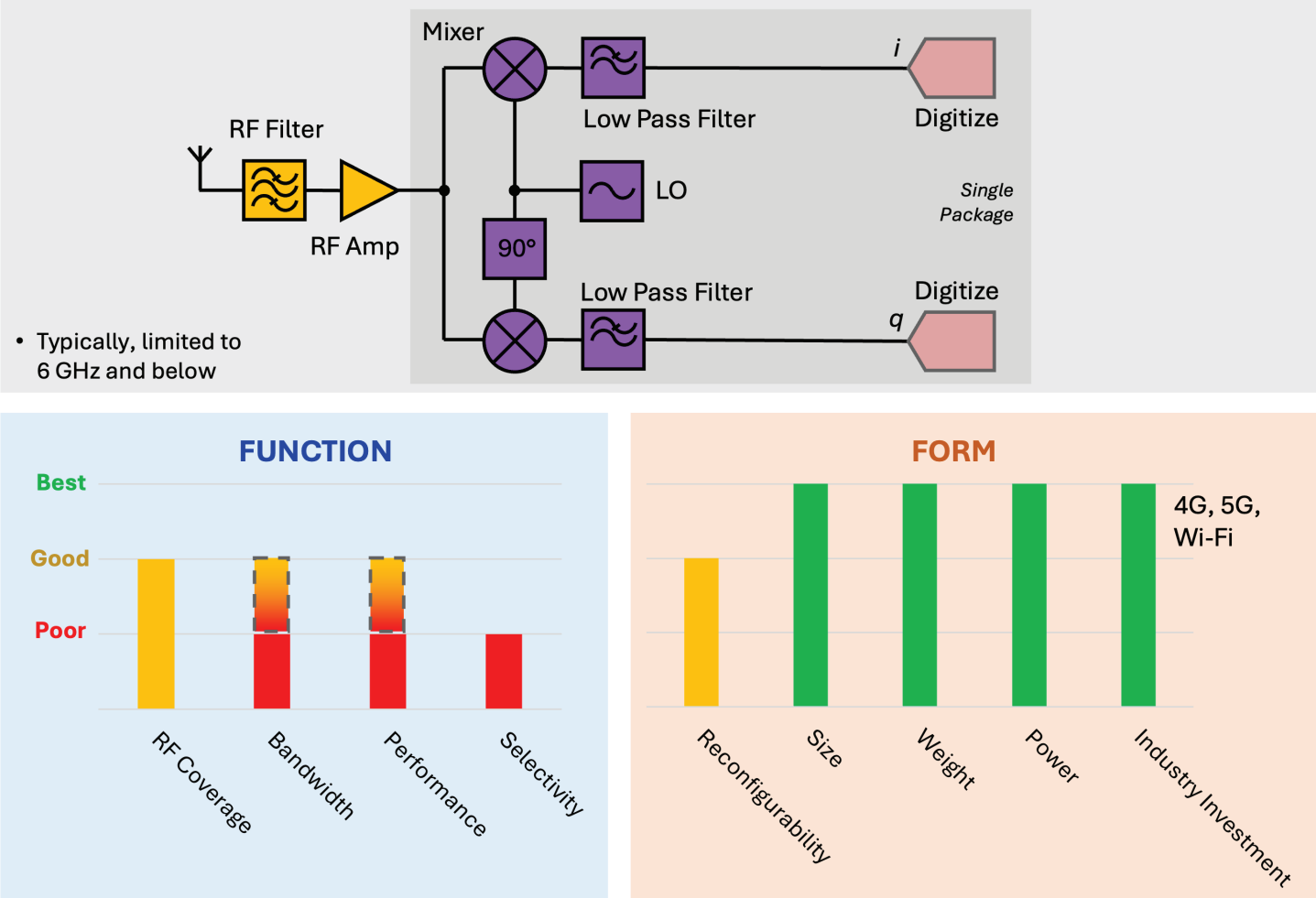


***Figure 8**: Form and Function for Zero IF architectures.*

Some of the lowest SWaP SDRs available are based on Zero IF architectures using RFICs. The lack of complex RF conversion stages, multiple local oscillators etc. make them very efficient on the RF side, all of which take up size, weight and power in some other approaches. They benefit from significant industry investment in semiconductors for applications such as cellular base stations, and Wi-Fi making them low cost, but do come with drawbacks. They are currently limited to a maximum frequency of about 6 GHz. They also suffer from being optimized for the applications driving their investment. For example, designers will have made trade-offs using assumptions about spectral interference, bandwidths etc. that might not be aligned with a more general use case. Overall they score better on Form than Function in our rating system. An example block diagram and some of Epiq's many products that are built on Zero IF are shown in **Figure 9**.

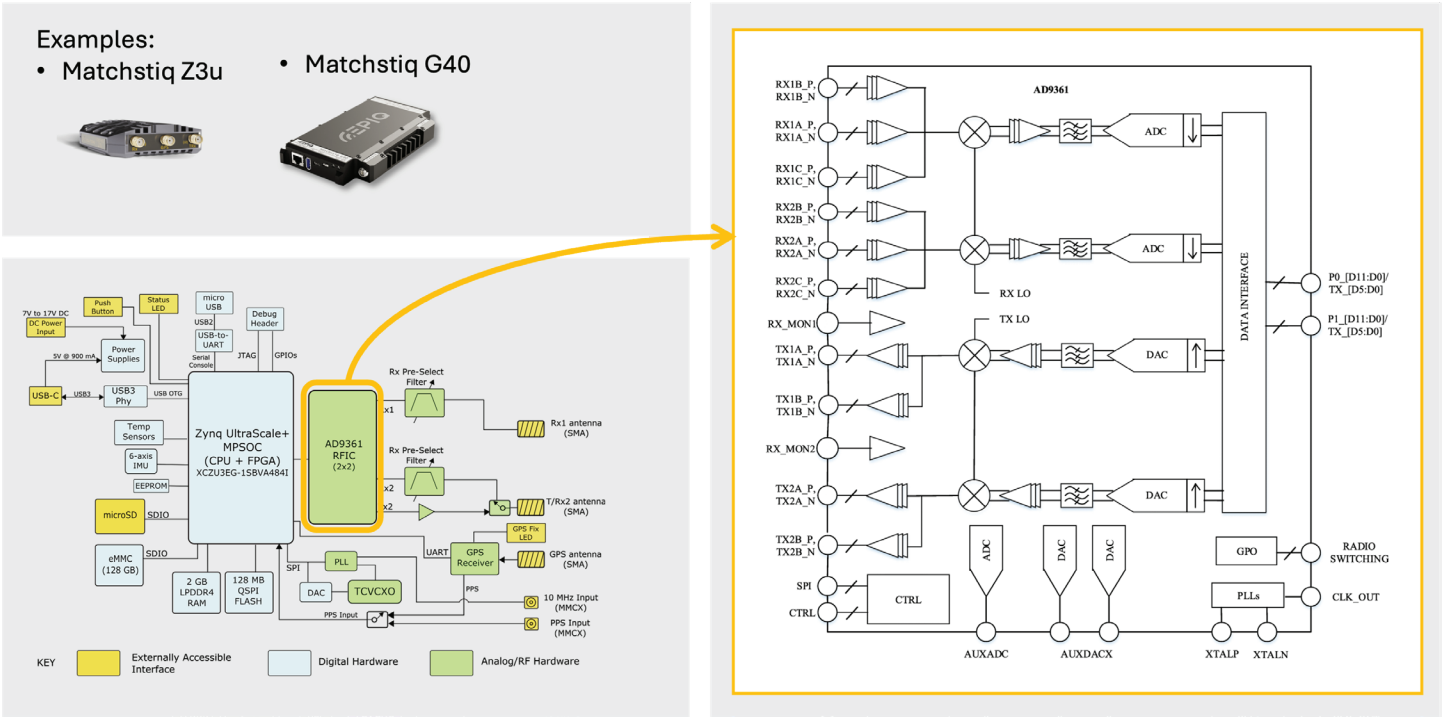


***Figure 9**: An example Zero IF RFSoC implemented in an SDR with its position alongside an CPU/ FPGA also shown. Many Epiq small form factor radios use this architecture, with two examples listed.*

Architecture 5: Combinations

Up to this point we have run through some common RF architectures and their pros and cons. A popular way of improving overall applicability and mitigating downsides is to combine architectures. This almost always means adding a block converter in front of one of the others, particularly when wishing to access higher frequency bands. We'll look at a couple of examples, and the benefits to Function and Form in doing so.

Example A: Block Conversion with Zero IF

Description	Block conversion allows access to frequencies higher than Zero IF can realize, while Zero IF keeps system SWaP footprint as low as possible.
Primary Benefit	Low SWaP, high frequency, moderate bandwidth approach.
Primary Cost	System performance is limited by Zero IF bandwidth & SFDR

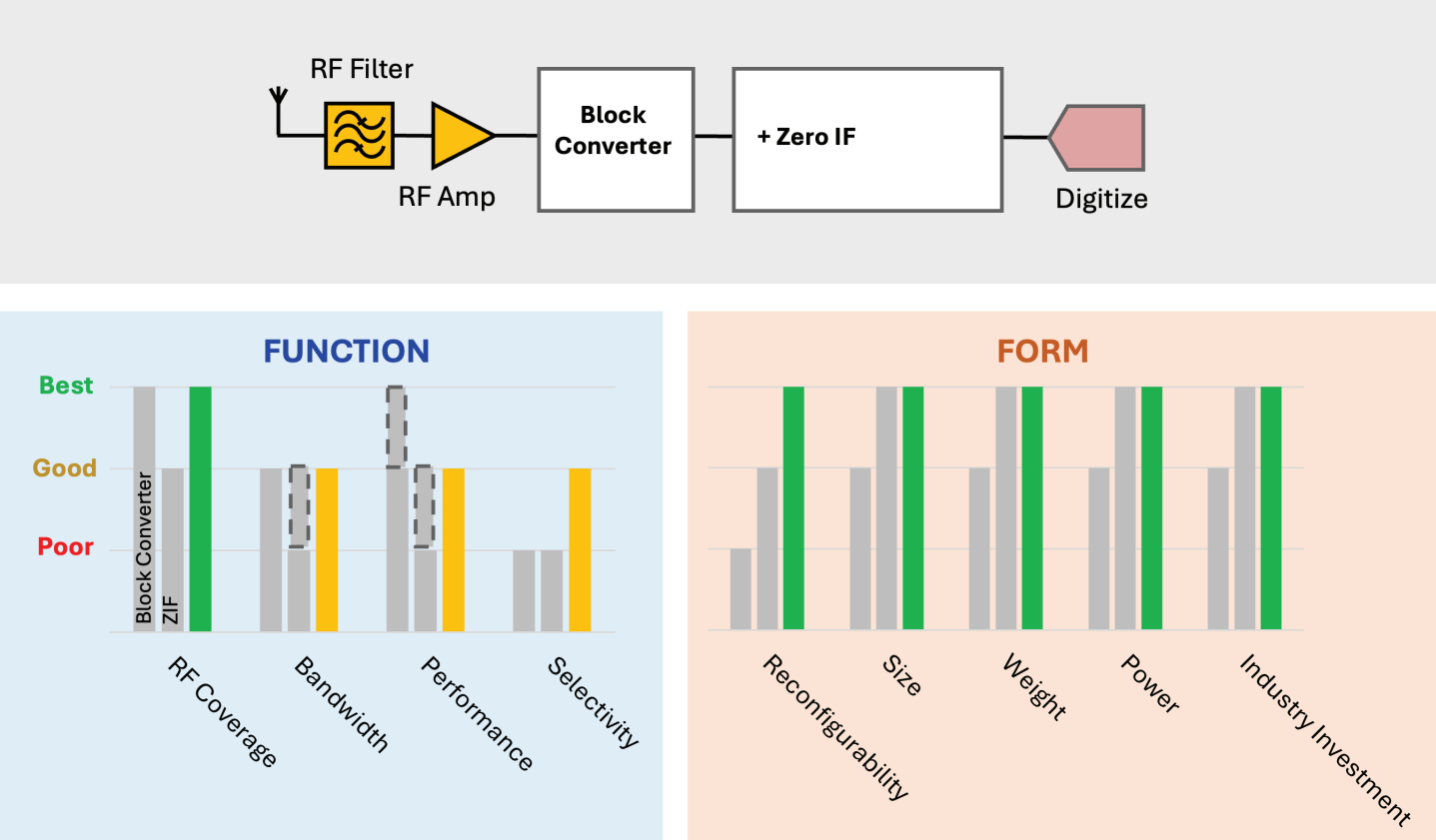


Figure 10: Form and Function for a combined block converter and Zero IF architecture.

Adding a block converter to a Zero IF architecture doesn't necessarily need to increase SWaP significantly, while it can increase flexibility and RF coverage. However, ultimately the RF performance will be most dependent upon the Zero IF part of the chain. For applications where RF signals of interest are geographically close, and SWaP is of high importance, such as UAS payloads, this can be an effective combination. The Epiq Matchstiq X40 shown in **Figure 11** is a good example.

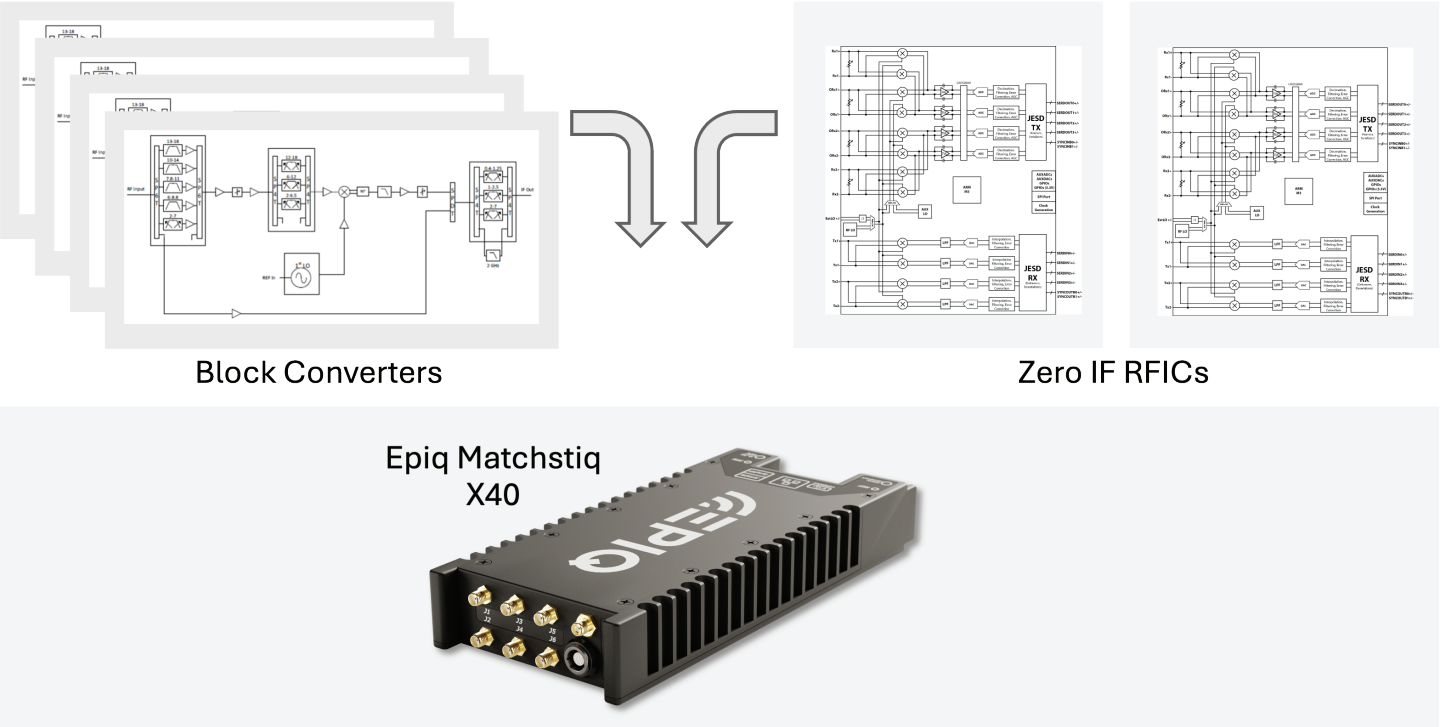
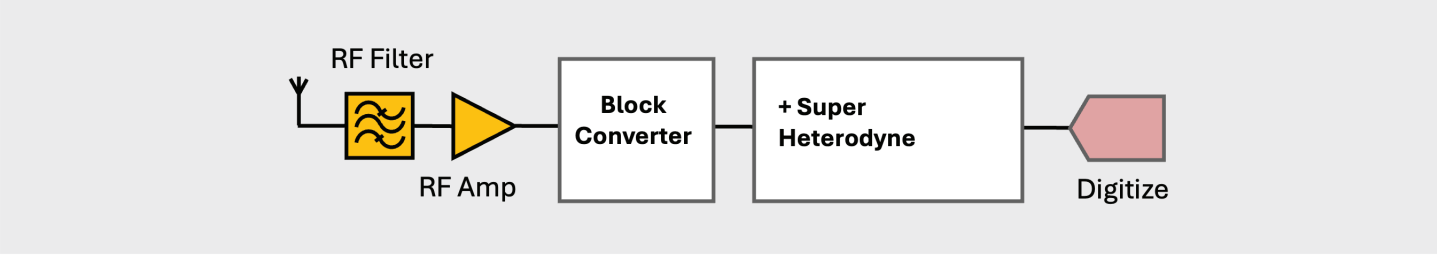
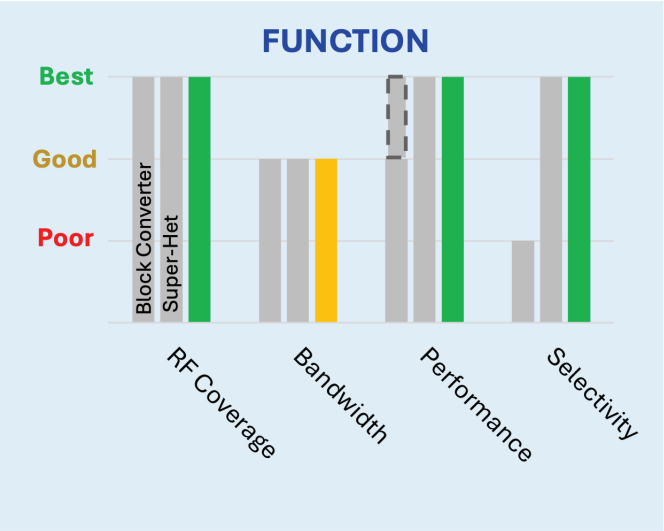


***Figure 11**: An example of a combined architecture, the Epiq X40 provides a seprate block converter to each of four receive channels. These are fed to two Zero IF RFIC blocks with two channels each. The combination enables RF access up to 18 GHz. Not shown is an additional block converter for the X40 transmit chain.*

Example B: Block Conversion with Superhet

Description	Extends superheterodyne architecture to mmW frequencies otherwise difficult to access with a pure heterodyne approach.
Primary Benefit	Highest performance architecture for ultra-wide RF access.
Primary Cost	Increased performance comes at the expense of SWaP.





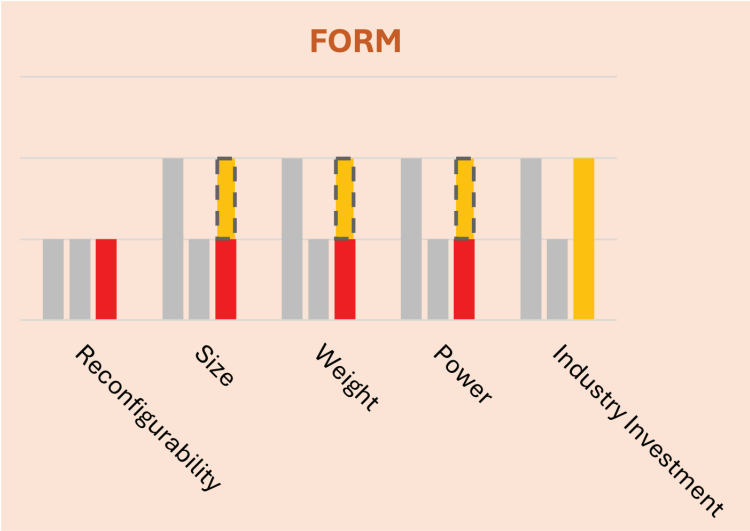


Figure 12: Form and Function for a combined block converter and Superhet architecture

For some applications needing extended frequency coverage, SWaP is less important than outright performance. This can be particularly true when signals of interest come from a long distance away and are in crowded spectrum with plenty of high-power interferers nearby. However, this approach is most effective when the block converter is of similarly high quality as the Superheterodyne SDR following it, otherwise performance is being wasted. An example of this approach is the NDR504 40 GHz, 4 channel downconverter, which is well matched to many 18 GHz Superheterodyne products from Epiq.

Pulling it All Together

Having looked at each case individually, what have we seen? **Figure 13** collects the Form/ Function charts into one picture. It becomes obvious that there is no one-size-fits-all approach, with different architectures proving beneficial solving particular sets of problems.

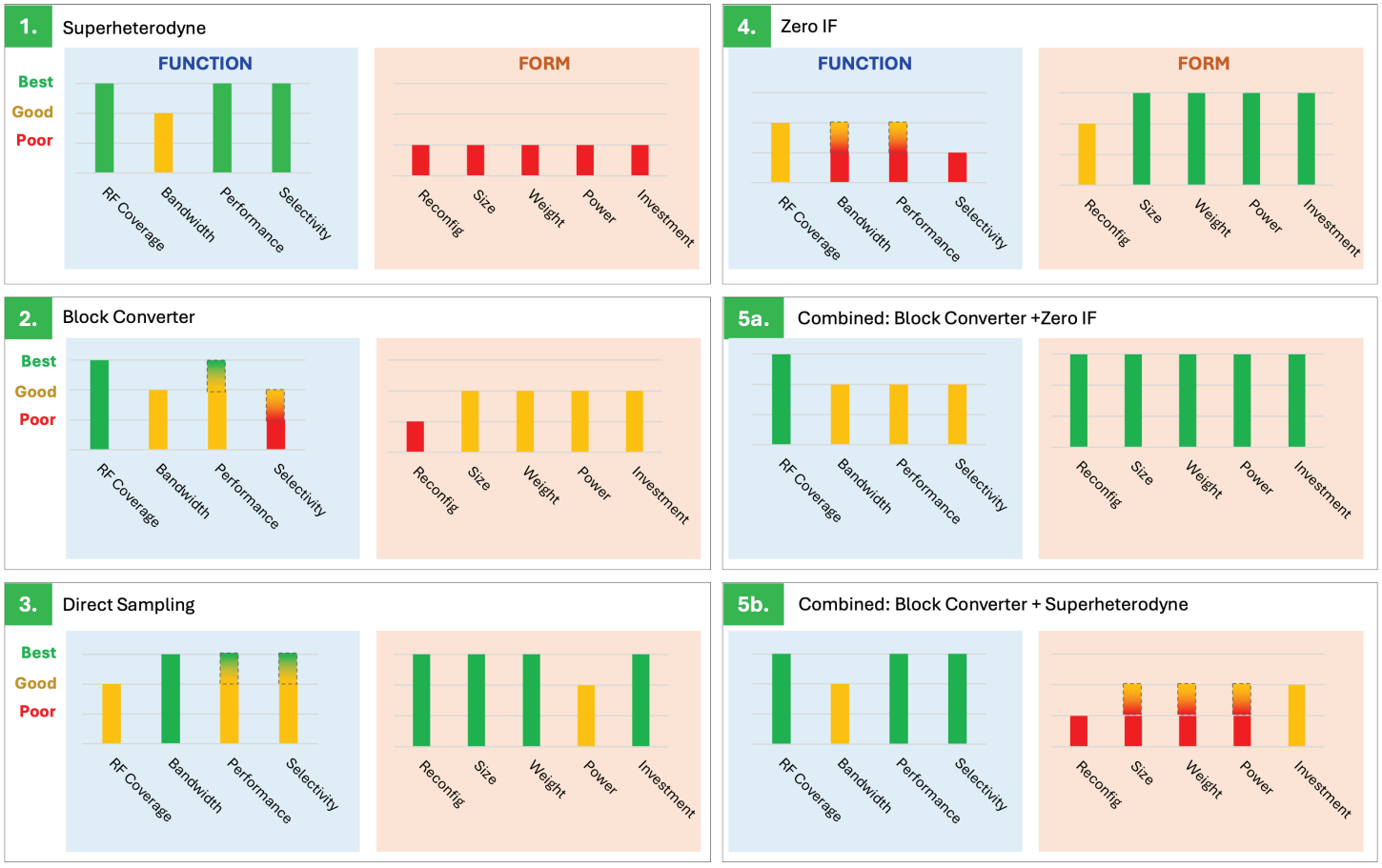


Figure 13: The Function and Form graphs for each architecture side-by-side for easy comparison

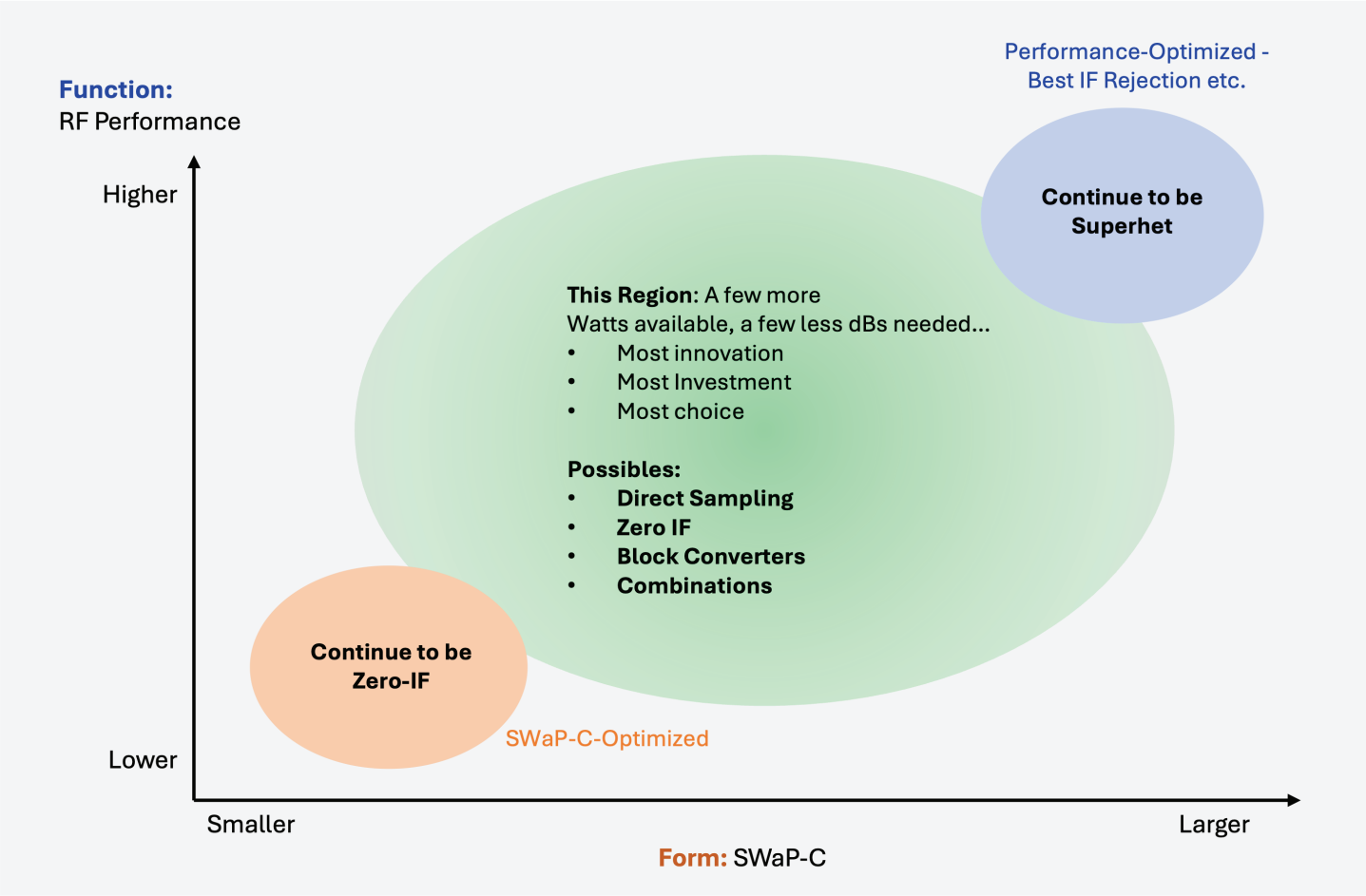


Figure 14: Function and Form regions with typical architecture choices expected going forward

If the lowest size, weight, power and cost are the overriding imperatives and lower RF coverage can be tolerated, Zero IF-based solutions look set to continue to be the architecture of choice. For the absolute best RF performance in difficult environments where higher SWaP-C can be tolerated, it seems likely that Superhets will continue to reign supreme. However, as shown in **Figure 14**, for situations where a few less dBs of performance are allowable, and/or a few more Watts of power etc., the sizable middle region of the graph is getting increasingly interesting. This is particularly true for direct sampling-based approaches, which are receiving significant investment and are evolving rapidly. For the sake of completeness, the typical maximum frequencies of the different architectures are also shown in **Figure 15**, and a small selection of useful references are given in **Further Reading**.

Overall, it is helpful to have multiple candidate RF architectures available to solve a particular combination of Form and Function requirements.

Architecture	Typical Maximum Frequency
Superhets	40 GHz+
Block Converters	40 GHz+
Direct Sampling	8 - 18 GHz depending upon implementation
Zero IF	6 GHz

Figure 15: Table showing typical maximum accessible frequencies for the four base architectures discussed while also maintaining good quality RF performance

Further Reading

The following is a brief sampling of references for many of the topics covered in this paper (live in August 2025).

1. Noise Spectral Density: A New ADC Metric?
   https://www.analog.com/en/resources/technical-articles/noise-spectral-density.html

2. Noise Spectral Density: A Better Way
   https://www.ti.com/lit/ab/sbaa625a/sbaa625a.pdf

3. Considering GS/s ADCs in RF Systems
   https://www.analog.com/en/resources/technical-articles/considering-GS/s-adcs-in-rf-systems.html

4. A Comparison on the Strengths of ZIF Architectures vs Direct RF Sampling:
   https://www.analog.com/en/resources/technical-articles/radio-architecture-matters.html

5. An Analysis of Sampling Spurs in Direct RF Sampling
   https://www.ti.com/lit/an/slaa824/slaa824.pdf

6. Quadrature Error Correction for Wideband Zero-IF Signals
   https://www.analog.com/en/resources/app-notes/an-2557.html

7. Superheterodyne Receivers
   https://www.microwaves101.com/encyclopedias/superheterodyne-receivers

Appendix A: Direct Sampling and Processing Gain

More information can be found in the Further Reading section as this note will be brief.

Direct Sampling benefits from Processing gain, which is realized through applying digital processing to a signal after it has been digitized to improve the signal-to-noise ratio (SNR).

When traditional analog-to-digital converters (ADCs) sample at 2x Nyquist for the bandwidth of interest, their noise is spread across the band of interest, also. The design of new high-speed ADCs which sample at ones to tens of Giga-Samples per second (GS/s) allows the sample rate to increase faster than noise increases. Decimation (digital filtering) reduces the processed noise while leaving the desired signal unchanged, improving SNR.

This is illustrated graphically in the sequence shown in **Figure 16** based on a simple experiment. A test signal generator tuned to 5.8 GHz was set to produce a single tone at a level of -10 dBm received inside the converter (1). The plots (2 to 9) show the signal, noise, and spurious products output by the converter under test.

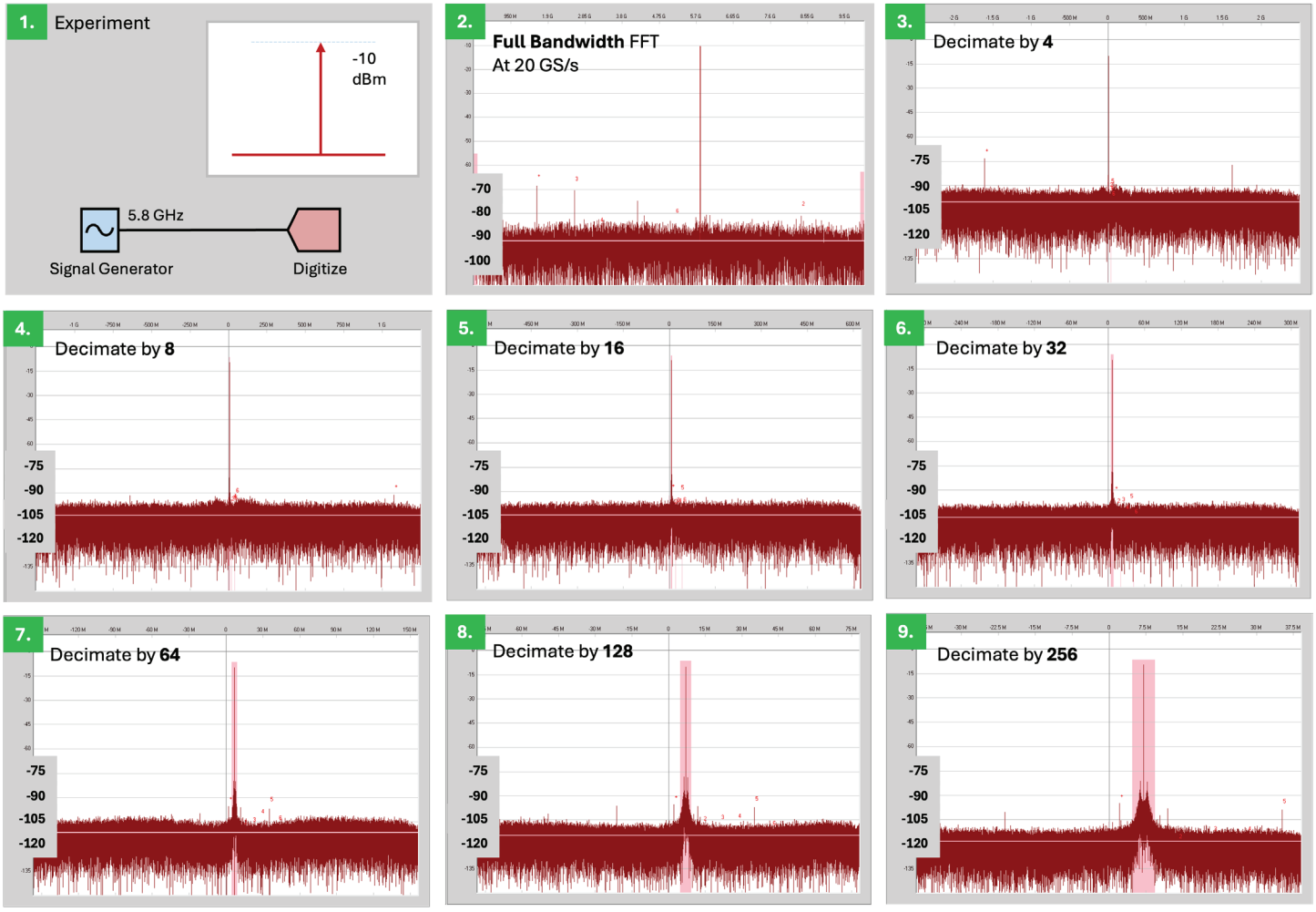
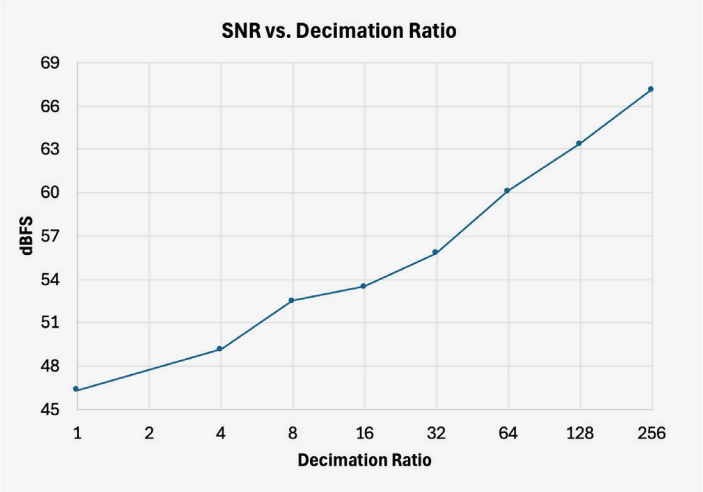


Figure 16: The experimental setup is shown in box 1, with results shown in subsequent boxes for increasing decimation factors. Note the drop in noise floor, and the variation in spur positions and magnitudes.



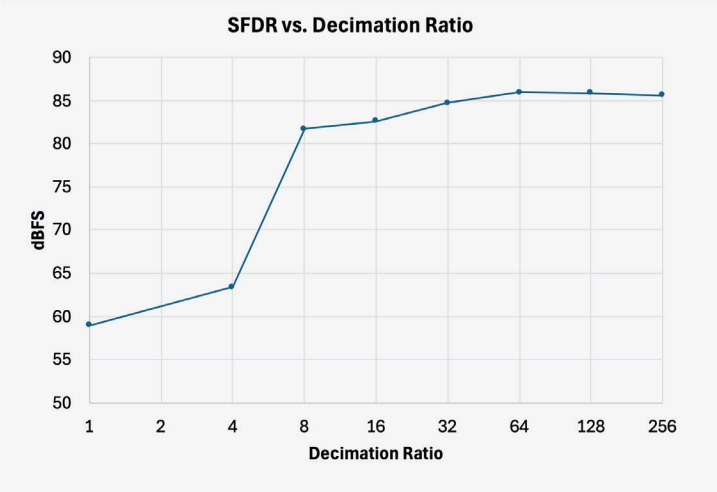


***Figure 17**: The results of the experiment above plotted graphically.*

More quantitatively, the plots in **Figure 17** show how the signal-to-noise ratio (SNR) on the left, and the spurious dynamic range (SFDR) on the right as the degree of decimation increases. For SNR, every decimation increase by 2 yields almost 3 dB of SNR improvement (loss in the digital filter usually makes it more like 2.9 dB). The change is SFDR is much less linear, and is driven by digital frequency planning and digitally filtering out Harmonic Distortion or Inter-Mod spurs that are limiting performance.

ABOUT EPIQ

Epiq Solutions develops cutting edge tools for engineering teams and government-focused organizations requiring situational awareness and detailed insight into their RF environments in order to identify and act against wireless threats.

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